

WHAT IS CLAIMED IS:

1. A semiconductor circuit comprising:
 - a first memory block having a plurality of first pairs of bit lines, a plurality of first word lines, and a plurality of first SRAM memory cells coupled to said plurality of first pairs of bit lines and first word lines;
 - a second memory block having a plurality of second pairs of bit lines, a plurality of second word lines, and a plurality of second SRAM memory cells coupled to said plurality of second pairs of bit lines and said second word lines;
 - a sense amplifier and a write amplifier;
 - a first pair of wiring lines coupled to said sense amplifier;
 - a second pair of wiring lines coupled to said write amplifier;
 - a first switch circuit which electrically connects one pair of said plurality of said first and second pairs of bit lines to said first pair of wiring lines; and
 - a second switch circuit which electrically connects one pair of said plurality of said first and second pairs of bit lines to said third pair of wiring lines,
 - wherein said first pair of wiring lines lies over said first and second memory block, and extends in a first direction of which said plurality of first pairs of bit lines and second pairs of bit lines extend,
 - wherein said second pair of wiring lines lies over said first and second memory block, and extends in said first direction,
 - wherein said first pair and second pairs of wiring lines are formed in a first metal layer,

wherein said plurality of first pairs of bit lines and second pairs of bit lines are formed in a second metal layer,

wherein read operations of said first and second SRAM memory cells are performed by using said first pair of wiring lines, and

wherein write operations of said first and second SRAM memory cells are performed by using said second pair of wiring lines.

2. The semiconductor circuit according to claim 1,
wherein a voltage between one pair of said plurality of first and second pairs of bit lines which is selected for a read operation is amplified by said sense amplifier.

3. The semiconductor circuit according to claim 2,
wherein said first and second pairs of wiring lines have an overlap in their operating period.

4. The semiconductor circuit according to claim 3,
wherein said overlap is to perform both read and write operations of one of said plurality of first and second SRAM memory cells.

5. The semiconductor circuit according to claim 2,
wherein said first switch circuit comprises a plurality of first MOSFETs, each having a source/drain path coupled between said first pair of wiring lines and each of said plurality of first pairs of bit lines, and a plurality of second MOSFETs, each

having a source/drain path coupled between said first pair of wiring lines and each of said plurality of second pairs of bit lines,

wherein said second switch circuit comprises a plurality of third MOSFETs, each having a source/drain path coupled between said second of wiring lines and each of said plurality of first pairs of bit lines, and a plurality of fourth MOSFETs, each having a source/drain path coupled between said second pair of wiring lines and each of said plurality of second pairs of bit lines.

6. The semiconductor circuit according to claim 5, further comprising:
a switch control circuit which outputs signals to control gates of said plurality of said first, second, third and fourth MOSFETs; and
a precharge circuit coupled to said first pair of wiring lines.

7. The semiconductor circuit according to claim 5, further comprising:
a switch control circuit which outputs signals to control gates of said plurality of said first, second, third and fourth MOSFETs;
a decoder circuit coupled to said plurality of said first and second word lines;
and
a precharge circuit coupled to said first pair of wiring lines,
wherein said first and second memory blocks are placed between said decoder circuit and said switch control circuit.

8. The semiconductor circuit according to claim 7, further comprising:
- a third memory block having a plurality of third pairs of bit lines, a plurality of third word lines, and a plurality of third SRAM memory cells coupled to said plurality of third pairs of bit lines and third word lines,
- wherein said plurality of first and third MOSFETs are placed between said first and second memory blocks, and
- wherein said plurality of second and fourth MOSFETs are placed between said second and third memory blocks.